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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

DANG, KHANH NMN

ART UNIT	PAPER NUMBER
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2111

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DATE MAILED: 04/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/870,808

Applicant(s)

BENNETT ET AL.

Examiner

Khanh Dang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 July 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-43 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-43 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a plurality of circuitries recited in claims 30-43 must be shown or the features canceled from the claims. Note that "circuitry" is a design of or a detailed plan for an electric circuit. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the plurality of circuitries recited in claims 30-43. Note that "circuitry" is a design of or a detailed plan for an electric circuit.

Claim Rejections - 35 USC § 112

Claims 1-43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claim 1, it is unclear from the language of the claim what may be "a split completion." The term "split completion" when taken out of context renders the claim indefinite. It is advised that the term "split completion" should be further defined in the claim.

With regard to claim 2, the essential structural cooperative relationships between a "split completion commitment limit register," "a total outstanding split completion register;" and "a next split completion size register" have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP 2172.01.

With regard to claim 9, it is unclear what may be the relationships between the "first split completion transaction arbiter" and the "second split completion transaction arbiter" with the "split completion transaction arbiter" specified in claim 1.

With regard to claim 10, the phrase "arbitrating the split completion" cannot be ascertained. Why arbitrating when there is only "a split completion." Further, it is unclear from the language of the claim what may be "a split completion." The term "split completion" when taken out of context renders the claim indefinite. It is advised that the term "split completion" should be further defined in the claim.

With regard to claim 15, the phrase "arbitrating the split completion" cannot be ascertained. Why arbitrating when there is only "a split completion."

With regard to claim 16, the phrase "arbitrating the split completion" cannot be ascertained. Why arbitrating when there is only "a split completion."

With regard to claim 23, the phrase "arbitrating the split completion" cannot be ascertained. Why arbitrating when there is only "a split completion." Further, it is unclear

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from the language of the claim what may be "a split completion." The term "split completion" when taken out of context renders the claim indefinite. It is advised that the term "split completion" should be further defined in the claim.

With regard to claim 28, the phrase "arbitrating the split completion" cannot be ascertained. Why arbitrating when there is only "a split completion."

With regard to claim 30, the essential structural cooperative relationships between a "buffer," "an arbiter," and "circuitry" have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP 2172.01. Further, it is unclear from the language of the claim what may be "a split completion." The term "split completion" when taken out of context renders the claim indefinite. It is advised that the term "split completion" should be further defined in the claim.

With regard to claim 33, it is unclear what may be the relationship between the "circuitry" in claim 33 and the "circuitry" cited in claims 30-32.

With regard to claim 34, it is unclear which circuitry the term "said circuitry" may refer to.

With regard to claim 39, the essential structural cooperative relationships between a "bridge" and a "processor" have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP 2172.01. Further, it is unclear from the language of the claim what may be "a split completion." The term "split completion" when taken out of context renders the claim indefinite. It is advised that the term "split completion" should be further defined in the claim.

With regard to claim 40, the essential structural cooperative relationships between the "circuitry" and the "bridge" and the "processor" (claim 39) have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP 2172.01.

With regard to claim 41, the essential structural cooperative relationships between the "circuitry" and the "bridge" and the "processor" (claim 39) have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP 2172.01.

With regard to claim 42, it is unclear what may be the relationship between the two circuitries recited in claim 42, and also their essential structural cooperative relationships with the "bridge" and the "processor" (claim 39) have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP 2172.01.

With regard to claim 43, it is unclear what may be the relationship between the "circuitry" in claim 43 and other recited circuitries. Further, the essential structural cooperative relationships between the "circuitry" in claim 43 and the "bridge" and the "processor" (claim 39) have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP 2172.01.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 7, 8, 10-18, 25-35, 37-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Shah.

At the outset, it is noted that similar claims will be grouped together to avoid repetition.

As broadly drafted, these claims do not define any structure/step that differs from Shah.

With regard to claims 1, 10, 11, 25, 30-33, Shah discloses an apparatus, comprising: a transaction facilitator (the PCI-X bus bridge of Shah, as any PCI-X bus bridge, must be in full compliance with PCI-X bus specification to include initiators or a so-called "transaction facilitator" for initializing the split transaction request and split completion request); a split-completion transaction arbiter (38, for example) coupled to the transaction facilitator; and a split-completion buffer (40, for example) coupled to the transaction facilitator. Also, according to PCI-X specification, all outstanding split completion transactions as well as the available space of the buffer must be monitored. In addition, according to the PCI-X bus specification, it is clear the quantity of split completion transactions must be limited to the size of the assigned buffer. See the

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widely available PCI-X Addendum to the PCI local Bus Specification, Revision 1.0a, 7/24/2000.

With regard to claim 3, it is clear that there is more than one bus coupled to said transaction facilitator.

With regard to claims 4 and 34, the PCI-X bus bridge of Shah, as any PCI-X bus bridge, must be in full compliance with PCI-X bus bridge specification to include initiators or a so-called "transaction facilitator" for initializing the split transaction request and split completion request. The initiator for initializing the transfer of a split completion is readable as a so-called "completer." See the widely available PCI-X Addendum to the PCI local Bus Specification, Revision 1.0a, 7/24/2000.

With regard to claims 5 and 35, in Shah, a "fair access" is determined by the arbiter 38.

With regard to claims 7 and 37, in Shah, a fixed-priority between the first and second priority levels can be determined by the arbiter 38.

With regard to claims 8 and 38, the PCI-X bus bridge of Shah, as any PCI-X bus bridge, must be in full compliance with PCI-X bus specification; wherein a target initiated latency limit is measured by a timer/counter, for example (a split completion transaction is originated from the target). See the widely available PCI-X Addendum to the PCI local Bus Specification, Revision 1.0a, 7/24/2000.

With regard to claims 12 and 26, the PCI-X bus bridge of Shah, as any PCI-X bus bridge, must be in full compliance with PCI-X bus specification. Thus, it is clear that a transaction must adhere to PCI-X sequence transaction protocol. In another word, in

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Shah, receiving a transaction comprises receiving part of an initiated sequence of transactions. With regard to claims 13 and 27, the PCI-X bus bridge of Shah, as any PCI-X bus bridge, must be in full compliance with PCI-X bus specification; wherein Sequence ID (Requester ID and tag, for example) must be used. In another word, it is clear that the transaction comprises a sequence identification and a command identification. See the widely available PCI-X Addendum to the PCI local Bus Specification, Revision 1.0a, 7/24/2000.

With regard to claims 14, 17, 18, and 29, the method of claim 13, the split completion transactions, according to the PCI-X bus specification, contain either read data or read completion message and comprise a sequence identification and a command identification.

With regard to claims 15 and 28, it is clear that arbitration process in Shah is based on priority ranking of the split completion transactions.

With regard to claim 16, the PCI-X bus bridge of Shah, as any PCI-X bus bridge, must be in full compliance with PCI-X bus specification; wherein a target initiated latency limit is provided (a split completion transaction is originated from the target). See the widely available PCI-X Addendum to the PCI local Bus Specification, Revision 1.0a, 7/24/2000.

With regard to claims 39-43, see explanation above.

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Claims 1-5, 7, 8, 10-35, 37-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Reams.

At the outset, it is noted that similar claims will be grouped together to avoid repetition.

As broadly drafted, these claims do not define any structure/step that differs from Reams.

With regard to claims 1, 10, 11, 25, 30-33, Reams discloses an apparatus, comprising: a transaction facilitator (the PCI-X bus bridge of Reams, as any PCI-X bus bridge, must be in full compliance with PCI-X bus specification to include initiators or a so-called "transaction facilitator" for initializing the split transaction request and split completion request); a split-completion transaction arbiter (18/118, for example) coupled to the transaction facilitator; and a split-completion buffer (PCI-X requires a buffer for storing split completion transactions) coupled to the transaction facilitator. Also, according to PCI-X specification, all outstanding split completion transactions as well as the available space of the buffer must be monitored. In addition, according to the PCI-X bus specification, it is clear the quantity of split completion transactions must be limited to the size of the assigned buffer. See the widely available PCI-X Addendum to the PCI local Bus Specification, Revision 1.0a, 7/24/2000.

With regard to claim 3, it is clear that there is more than one bus coupled to said transaction facilitator.

With regard to claims 4 and 34, the PCI-X bus bridge of Reams, as any PCI-X bus bridge, must be in full compliance with PCI-X bus bridge specification to include

initiators or a so-called "transaction facilitator" for initializing the split transaction request and split completion request. The initiator for initializing the transfer of a split completion is readable as a so-called "completer." See the widely available PCI-X Addendum to the PCI local Bus Specification, Revision 1.0a, 7/24/2000.

With regard to claims 5 and 35, it is clear that in Reams, a "fair access" is determined by the arbiter 18/118.

With regard to claims 7 and 37, in Reams, a fixed-priority between the priority levels can be determined by the arbiter 18/118.

With regard to claims 8 and 38, the PCI-X bus bridge of Reams, as any PCI-X bus bridge, must be in full compliance with PCI-X bus specification; wherein a target initiated latency limit is measured by a timer/counter, for example (a split completion transaction is originated from the target).

With regard to claims 12 and 26, the PCI-X bus bridge of Reams, as any PCI-X bus bridge, must be in full compliance with PCI-X bus specification. Thus, it is clear that a transaction must adhere to PCI-X sequence transaction protocol. In another word, in Reams, receiving a transaction comprises receiving part of an initiated sequence of transactions. With regard to claims 13 and 27, the PCI-X bus bridge of Reams, as any PCI-X bus bridge, must be in full compliance with PCI-X bus specification; wherein Sequence ID (Requester ID and tag, for example) must be used. In another word, it is clear that the transaction comprises a sequence identification and a command identification. See the widely available PCI-X Addendum to the PCI local Bus Specification, Revision 1.0a, 7/24/2000.

With regard to claims 14, 17, 18, and 29, the method of claim 13, the split completion transactions, according to the PCI-X bus specification, contain either read data or read completion message and comprise a sequence identification and a command identification.

With regard to claims 15 and 28, it is clear that arbitration process in Reams is based on priority ranking of the split completion transactions.

With regard to claim 16, the PCI-X bus bridge of Reams, as any PCI-X bus bridge, must be in full compliance with PCI-X bus specification; wherein a target initiated latency limit is provided (a split completion transaction is originated from the target).

With regard to claim 19, Reams discloses a system, comprising: a requester (12); an arbiter bridge (comprising arbiter 18) coupled to said requester (12); a microprocessor (controller 16) coupled to said arbiter bridge (comprising arbiter 18); and a target device (13) coupled to said arbiter bridge (comprising arbiter 18).

With regard to claim 20, the system further comprises a bus arbiter (18) coupled to said arbiter bridge.

With regard to claim 21, it is clear that the requester (13) comprises a microprocessor coupled to said arbiter bridge (comprising arbiter 18).

With regard to claim 22, unlike PCI bus, PCI-X requires split transactions, it is clear from at least Fig. 2 that the system of Reams employs PCI-X protocol. Thus, according the PCI-X specification, there must be initiators or a so-called "transaction facilitator" for initializing the split transaction request and split completion request. It is also clear that

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the PCI-X bus bridge of Reams, as any PCI-X bus bridge, must be in full compliance with PCI-X bus specification. Thus, it is clear that a transaction must adhere to PCI-X sequence transaction protocol. See the widely available PCI-X Addendum to the PCI local Bus Specification, Revision 1.0a, 7/24/2000.

With regard to claim 23, see explanation regarding to claim 22. Note also that PCI-X specification requires a buffer for storing split completion transactions.

With regard to claim 24, the target device comprises a memory device (memory module) coupled to said arbiter bridge.

With regard to claims 39-43, see explanation above.

Claims 1-5, 7-35, 37-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Fischer.

At the outset, it is noted that similar claims will be grouped together to avoid repetition.

As broadly drafted, these claims do not define any structure/step that differs from Fischer.

With regard to claims 1, 10, 11, 25, 30-33, Fischer discloses an apparatus, comprising: a transaction facilitator (62/64, for example); a split-completion transaction arbiter (162, for example) coupled to the transaction facilitator (62/64, for example); and a split-completion buffer (data registers included in data path logic 106) coupled to the transaction facilitator. Also, according to PCI-X specification, all outstanding split completion transactions as well as the available space of the buffer must be monitored.

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In addition, according to the PCI-X bus specification, it is clear the quantity of split completion transactions must be limited to the size of the assigned buffer. See the widely available PCI-X Addendum to the PCI local Bus Specification, Revision 1.0a, 7/24/2000.

With regard to claim 3, it is clear that there is more than one bus (bus for 60 and bus for 62) coupled to said transaction facilitator.

With regard to claims 4 and 34, in Fischer, the transaction facilitator comprises an initiator (22) and a completer (initiator 22 of the responder for initializing a split completion transaction).

With regard to claims 5, 7, 35, 37, it is clear that arbitration is based on a fixed priority.

With regard to claims 8 and 38, the PCI-X bus bridge of Fischer, as any PCI-X bus bridge, must be in full compliance with PCI-X bus specification; wherein a target initiated latency limit is measured by a counter, for example (a split completion transaction is originated from the target). See the widely available PCI-X Addendum to the PCI local Bus Specification, Revision 1.0a, 7/24/2000.

With regard to claim 9, see Figs. 2, 8, and 9, and description thereof. Note particularly arbiters 160 and 162.

With regard to claims 12, and 26, the PCI-X bus bridge of Fischer, as any PCI-X bus bridge, must be in full compliance with PCI-X bus specification. Thus, it is clear that a transaction must adhere to PCI-X sequence transaction protocol. In another word, in Shah, receiving a transaction comprises receiving part of an initiated sequence of

transactions. See the widely available PCI-X Addendum to the PCI local Bus Specification, Revision 1.0a, 7/24/2000.

With regard to claim 13, and 27, the PCI-X bus bridge of Fischer, as any PCI-X bus bridge, must be in full compliance with PCI-X bus specification; wherein Sequence ID (Requester ID and tag, for example) must be used. In another word, it is clear that the transaction comprises a sequence identification and a command identification. See the widely available PCI-X Addendum to the PCI local Bus Specification, Revision 1.0a, 7/24/2000. See the widely available PCI-X Addendum to the PCI local Bus Specification, Revision 1.0a, 7/24/2000.

With regard to claims 14, 17, 18, and 29, the split completion transactions, according to the PCI-X bus specification, contain either read data or read completion message and comprise a sequence identification and a command identification. See the widely available PCI-X Addendum to the PCI local Bus Specification, Revision 1.0a, 7/24/2000.

With regard to claims 15 and 28, it is clear that arbitration process in Fischer is based on priority ranking of the split completion transactions.

With regard to claim 16, the PCI-X bus bridge of Fischer, as any PCI-X bus bridge, must be in full compliance with PCI-X bus specification; wherein a target initiated latency limit is provided (a split completion transaction is originated from the target). See the widely available PCI-X Addendum to the PCI local Bus Specification, Revision 1.0a, 7/24/2000.

With regard to claim 19, Fischer discloses a system comprising: a requester (60); an arbiter bridge (shown generally in Fig. 2 coupled the initiator 60 to the responder 62) coupled to said requester (60); a microprocessor (transfer controller 109, for example) coupled to said arbiter bridge; and a target device (62) coupled to said arbiter bridge.

With regard to claim 20, the system of Fischer further comprises a bus arbiter (160/162) coupled to said arbiter bridge.

With regard to claim 21, the requester (60) comprises a second microprocessor (52) coupled to said arbiter bridge.

With regard to claim 22, the requester comprises: a sequence initiator (22 of 62) coupled to said arbiter bridge; and a sequence requester (22 of 60) coupled to said arbiter bridge.

With regard to claim 23, unlike PCI bus, PCI-X requires split transactions, it is clear from at least Fig. 2 that the system of Reams employs PCI-X protocol. Thus, according the PCI-X specification, there must be initiators or a so-called "transaction facilitator" for initializing the split transaction request and split completion request. It is also clear that the PCI-X bus bridge of Reams, as any PCI-X bus bridge, must be in full compliance with PCI-X bus specification. Thus, it is clear that a transaction must adhere to PCI-X sequence transaction protocol. See the widely available PCI-X Addendum to the PCI local Bus Specification, Revision 1.0a, 7/24/2000.

With regard to claim 24, the target device comprises a memory device (memory module) coupled to said arbiter bridge.

With regard to claims 39-43, see explanation above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shah.

Shah, as explained above, discloses the claimed invention including the use of priority arbitration. Shah does not disclose specifically the use of round robin (rotating) arbitration. However, arbitration based on round robin (rotating) is old and well-known in the art as evidenced by at least Bennett (cited under relevant art). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use arbitration based on round robin fashion, since the Examiner takes Official Notice that arbitration based on round robin is old and well-known; and using arbitration based on round robin fashion in Shah's arbitration only involves ordinary skill in the art.

Claims 6 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reams.

Reams, as explained above, discloses the claimed invention including the use of priority arbitration. Reams does not disclose specifically the use of round robin (rotating) arbitration. However, arbitration based on round robin (rotating) is old and well-known in

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the art as evidenced by at least Bennett (cited under relevant art). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use arbitration based on round robin fashion, since the Examiner takes Official Notice that arbitration based on round robin is old and well-known; and using arbitration based on round robin fashion in Reams' arbitration only involves ordinary skill in the art.

Claims 6 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer.

Fischer, as explained above, discloses the claimed invention including the use of priority arbitration. Fischer does not disclose specifically the use of round robin (rotating) arbitration. However, arbitration based on round robin (rotating) is old and well-known in the art as evidenced by at least Bennett (cited under relevant art). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use arbitration based on round robin fashion, since the Examiner takes Official Notice that arbitration based on round robin is old and well-known; and using arbitration based on round robin fashion in Fischer's arbitration only involves ordinary skill in the art.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shah in view of Kelley et al.

Shah, as explained above, discloses the claimed invention except for the use of a plurality of registers as recited in claim 2. Kelley et al. disclose the use of a plurality of

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registers. Specifically, Kelley discloses the use of register 215/217 readable as "a split completion commitment limit register"; register 211/213 readable as a "total outstanding split completion register;" and register 231/233 readable as a "next split completion size register." It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Shah with a plurality of registers, as taught by Kelley et al., for the purpose of providing an improved methodology and implementing system which enables a more advantageous use of buffer availability in transferring information between devices connected within an information processing system.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reams in view of Kelley et al.

Reams, as explained above, discloses the claimed invention except for the use of a plurality of registers as recited in claim 2. Kelley et al. disclose the use of a plurality of registers. Specifically, Kelley discloses the use of register 215/217 readable as "a split completion commitment limit register"; register 211/213 readable as a "total outstanding split completion register;" and register 231/233 readable as a "next split completion size register." It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Reams with a plurality of registers, as taught by Kelley et al., for the purpose of providing an improved methodology and implementing system which enables a more advantageous use of buffer availability in transferring information between devices connected within an information processing system.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer in view of Kelley et al. (6,457,077)

Fischer, as explained above, discloses the claimed invention except for the use of a plurality of registers as recited in claim 2. Kelley et al. disclose the use of a plurality of registers. Specifically, Kelley discloses the use of register 215/217 readable as "a split completion commitment limit register"; register 211/213 readable as a "total outstanding split completion register;" and register 231/233 readable as a "next split completion size register." It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Fischer with a plurality of registers, as taught by Kelley et al., for the purpose of providing an improved methodology and implementing system which enables a more advantageous use of buffer availability in transferring information between devices connected within an information processing system.

U.S. Patent Nos. 6,697,904 to Bennett, 6,425,024 to Kelley et al., 6,581,141 to Kelley et al., 6,694,397 to Lackey, Jr. et al., and 6,647,454 to Solomon are of particular interest and cited as relevant art.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.



Khanh Dang
Primary Examiner